Curriculum Vitae – Francesco Maria Puglisi

Francesco Maria Puglisi
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Scopus: https://www.scopus.com/authid/detail.uri?origin=resultslist&authorId=55512692700

BIOGRAPHY AND SHORT C.V.

Francesco Maria Puglisi was born in [redacted].

[2008] **Bachelor Degree in Electronic Engineering** from "Università della Calabria", full marks with honors. Thesis title: "Sistema di Ausilio per Persone Ipoudenti Easywearable Basato su Filtri Digitali Programmabili: Microcontrollore e DAC". Advisor: Prof. [redacted].
[2010] **Visiting Master Student at imec**, Belgium. Supervisor: Dr. [redacted] (imec, Belgium).
[2010] **Master Degree in Microelectronic Engineering** from "Università della Calabria", full marks with honors. Thesis title: "Separation of Bulk Lifetime and Surface Recombination Velocities in Silicon Solar Cells: an In-Line, Low-Cost, and Non-Destructive Technique". Advisors: Prof. [redacted] (Università della Calabria), Dr. [redacted] (imec, Belgium).
[2011] Professional Practice Exam ("Esame di Stato") – I.C.T. Engineer.
[2012] **Admitted to the Ph.D. school (XXVII cycle) in Information and Communication Technology (I.C.T.)** – Electronics and Telecommunications at "Università di Modena e Reggio Emilia". Advisor: Prof. [redacted].
[2013] **Visiting Ph.D. Student at "SEMATECH", Albany (N.Y.), U.S.A.** Advisor: Dr. [redacted].
[2015] **Ph.D. degree in I.C.T. from "Università di Modena e Reggio Emilia", full marks**. Thesis title: "A Unified Understanding of HfO_2-RRAM Operations: Modeling and Reliability". Advisor: Prof. [redacted]
[2015] (to 2018**) Post-Doc Researcher** ("Assegnista di Ricerca") at "Università di Modena e Reggio Emilia".
[2016] **Adjunct Professor**, "Advanced Electron Devices" course, "Università di Modena e Reggio Emilia", academic year 2015-2016.
[2017] **Adjunct Professor**, "Micro and Nano Electronics" course, "Università di Modena e Reggio Emilia", academic year 2017-2018.
[2017] National Academic Qualification as Associate Professor ("Abilitazione Scientifica Nazionale alle Funzioni di Professore di Seconda Fascia"), S.C. 09/E3 Elettronica.
[2018] **Associate Professor of Electronics at "Università di Modena e Reggio Emilia"**.

RESEARCH INTERESTS

- **Device characterization**, electrical characterization of RRAM, FTJ, and FeFET devices (operation, variability, and reliability); noise characterization and advanced data analysis in emerging NVMs, silicon FinFETs, and ultra-thin dielectric films; electrical measurements for defects characterization; characterization for reliability of silicon FinFETs, compound semiconductor devices, and advanced bipolar transistors; characterization of 2D devices.

- **Device and circuit modeling and simulation**, physics-based and compact modeling of RRAM and FTJ devices, with emphasis on Random Telegraph Noise (RTN); simulations of charge transport, charge

trapping, and breakdown in dielectrics and ferroelectrics; TCAD simulations for variability and reliability of compound semiconductor devices for logic; simulation of advanced devices with 2D materials.

- **Circuits and architectures for new computing paradigms**, circuit design for advanced non Von-Neumann and bio-inspired edge computing architectures such as Binary and Spiking Neural Networks; Logic-in-Memory (LiM) computing schemes; circuits for advanced data encryption such as RTN-based true random number generators and physical unclonable functions.

AWARDS AND SCIENTIFIC SOCIETY MEMBERSHIPS

- Recipient of the "Best Student Paper Award" at the ICICDT (International Conference on IC Design and Technology) 2013, Pavia (Italy), 29-31.05.2013, for the paper "A Compact Model of Hafnium-Oxide-Based Resistive Random Access Memory".
- Recipient of the "Distinguished International Researcher Certificate" assigned twice by the Rector of the "Università di Modena e Reggio Emilia", Prof. [redacted], on January 13th 2014 and on December 15th 2017.
- Recipient of the "Best Ph.D. Dissertation Award 2015" for the best Ph.D. Thesis in I.C.T. at the "Università di Modena e Reggio Emilia" discussed in 2015.
- Recipient of the "Best Paper Award" at the ESSDERC (46th European Solid-State Device Research Conference) 2016, Lausanne (Switzerland), 12-15.09.2016, for the paper "Probing Defects Generation During Stress in High-k/Metal Gate FinFETs by Random Telegraph Noise Characterization".
- Recipient of the "Best Oral Presentation Award" at the Riunione Annuale GE (Gruppo Italiano di Elettronica) 2016, Brescia (Italy), 22-24.06.2016, for the paper "Effects of Border Traps on Hysteresis and Mobility Measurement in InGaAs Quantum-Well MOSFETs".
- Recipient of the "Best Paper Award" at the ESSDERC (49th European Solid-State Device Research Conference) 2019, Karkow (Poland), 23-26.09.2019, for the paper "SIMPLY: Design of a RRAM-Based Smart Logic-in-Memory Architecture using RRAM Compact Model".
- Co-recipient of the "Best Student Paper Award" at the IEEE IIRW (International Integrated Reliability Workshop) 2020, Fallen Leaf Lake, California (U.S.A.), 04-29.10.2020, for the paper "Circuit Reliability Analysis of In-Memory Inference in Binarized Neural Networks".
- Recipient of the A.I.C.I. (Associazione Italiana Coniugi Ingegneri) "E. Loizzo Memorial Award" assigned at the best graduate student in Engineering at the "Università della Calabria" during the 2010-2012 timeframe.
- IEEE Student Member (2012-2014), Member (2015-Today).
- Member of IEEE Young Professionals (2015-Today).
- Member of IEEE Electron Device Society (2018).
- Member of SIE - Società Italiana di Elettronica (2013-Today).

TEACHING AND STUDENT MENTORING

Teaching:

- Instructor of undergraduate- and graduate-level courses in Electronics in the following fields: semiconductor devices, analog electronics, basic digital circuits, advanced electron devices, reliability.

Student Mentoring:

- Advisor /co-advisor of 13 thesis works of master (12) and bachelor (3) students.
- Advisor /co-advisor of 3 Ph.D. students and several early stage researchers.

- Member of the International Ph.D. Dissertation Committee, Ph.D. Degree in Electronics, Candidate: [redacted], December 2020, Technical University of Wien, Austria.
- Member of the International Ph.D. Dissertation Committee, Ph.D. Degree in Nanosciences – Research Direction: Electronic Engineering, Candidate: [redacted] July 2018, University of Barcelona, Spain.
- Member of the International Ph.D. Dissertation Committee, Ph.D. Degree in "Scienze e Ingegneria dell'Ambiente delle Costruzioni e dell'Energia", May 2019, University of Calabria, Italy.

INVITED TALKS

- 2016, IEEE International Integrated Reliability Workshop (IIRW), Fallen Leaf Lake, California, U.S.A.
- 2017, IEEE International Symposium on the Physical and Failure Analysis of Integrated Circuits (IPFA), Chengdu, China.
- 2017, ChinaRRAM, Suzhou, China.
- 2017, Non-Volatile Memory Technology Symposium (NVMTS), Aachen, Germany.
- 2018, International Conferences on Modern Materials and Technologies (CIMTEC), Perugia, Italy.
- 2021, IEEE International Symposium on the Physical and Failure Analysis of Integrated Circuits (IPFA) – virtual – Singapore.

CONFERENCE COMMITTEES AND PEER REVIEW

- **IEEE European Solid-State Device Research Conference (ESSDERC)**
  - 2022, Technical Program Co-Chair – Technical Program Committee Member
  - 2021, Technical Program Committee Member
  - 2020, Technical Program Committee Member

- **IEEE International Integrated Reliability Workshop (IIRW)**
  - 2022, Technical Program Chair
  - 2021, Vice Technical Program Chair, Tutorials Co-Chair, and Technical Program Committee Member
  - 2020, Publication Chair, Vice Technical Program Chair, and Technical Program Committee Member
  - 2019, Publication Chair and Technical Program Committee Member
  - 2018, European Liaison and Technical Program Committee Member
  - 2017, Technical Program Committee Member

- **IEEE International Reliability Physics Symposium (IRPS)**
  - 2022, Emeritus Track Chair (Gate/MOL Dielectrics)
  - 2021, Track Chair (Gate/MOL Dielectrics)
  - 2020, Track Vice-Chair (Gate/MOL Dielectrics)
  - 2019, Technical Program Committee Member (Gate/MOL Dielectrics)
  - 2018, Technical Program Committee Member (Gate/MOL Dielectrics)
  - 2017, Technical Program Committee Member (Gate/MOL Dielectrics)

- **IEEE International Symposium on the Physical and Failure Analysis of Integrated Circuits (IPFA)**
  - 2021, Track Chair (Emerging Topic in FA and Reliability)
  - 2020, Track Chair (Emerging Topic in FA and Reliability)
  - 2019, Technical Program Committee Member (Emerging Topic in FA and Reliability)
  - 2018, Technical Program Committee Member (Emerging Topic in FA and Reliability)
  - 2017, Technical Program Committee Member and Session Chair (Emerging Topics in FA and Reliability)

- **IEEE Electron Devices Technology and Manufacturing (EDTM)**
    - 2022, Technical Program Committee Member (Reliability)

- **First International Conference on Microelectronic Devices and Technologies (MicDAT)**
    - 2018, Technical Program Committee Member

- **China RRAM International Workshop (ChinaRRAM)**
    - 2017, Technical Program Committee Member

- **Reviewer for the following journal (non-exhaustive list)**: NPG Nature Electronics, NPG Nature Communications, NPG Scientific Reports, IEEE Electron Device Letters (Golden Reviewer), IEEE Transactions on Electron Devices (Golden Reviewer), IEEE Transactions on Device and Materials Reliability, IEEE Journal of Electron Device Society, IEEE Journal on Selected and Emerging Topics in Circuits and Systems, AIP Applied Physics Letters, AIP Journal of Applied Physics, Solid-State Electronics, 2D Materials, Journal of Vacuum Science and Technology, Microelectronic Engineering, Microelectronics Reliability.

- **Associate Editor** for the Hardware-related topics in **Frontiers in Computational Neuroscience**
- **Guest Editor** for the **Brain-Inspired Computing: Neuroscience Drives the Development of New Electronics and Artificial Intelligence** to appear in **Frontiers**

- **Co-organizer** of the **Brain-Inspired Computing Workshop** held in Modena (Italy) in 2019 and 2021

SELECTED RECENT PUBLICATIONS

Co-author of > 100 publications, h-index of 20 (Google Scholar) 17 (Scopus)

[1] Pan, C. B., Ji, Y. F., Xiao, N., Hui, F., Tang, K., Guo, Y., Xie, X., Puglisi, F. M., Larcher, L., Miranda, E., Jiang, L. L., Shi, Y. Y., Valov, I., McIntyre, P. C., Waser, R., Lanza, M., "Coexistence of Grain-Boundaries-Assisted Bipolar and Threshold Resistive Switching in Multilayer Hexagonal Boron Nitride". Adv. Funct. Mater. 2017, 27, 1604811.

[2] Wen, C., Li, X., Zanotti, T., Puglisi, F. M., Shi, Y., Saiz, F., Antidormi, A., Roche, S., Zheng, W., Liang, X., Hu, J., Duhm, S., Roldan, J. B., Wu, T., Chen, V., Pop, E., Garrido, B., Zhu, K., Hui, F., Lanza, M., "Advanced Data Encryption using 2D Materials", Adv. Mater. 2021, 33, 2100185. https://doi.org/10.1002/adma.202100185 – **cited in the Nature Electronics research highlights of June 2021** available at: https://www.nature.com/articles/s41928-021-00608-7

[3] Zanotti T, Puglisi FM, Pavan P., "Energy-Efficient Non-Von Neumann Computing Architecture Supporting Multiple Computing Paradigms for Logic and Binarized Neural Networks". Journal of Low Power Electronics and Applications. 2021; 11(3):29. https://doi.org/10.3390/jlpea11030029

[4] Li, X., Zanotti, T., Wang, T., Zhu, K., Puglisi, F. M., Lanza, M., "Random Telegraph Noise in Metal-Oxide Memristors for True Random Number Generators: A Materials Study". Adv. Funct. Mater. 2021, 31, 2102172. https://doi.org/10.1002/adfm.202102172

[5] T. Zanotti, F. M. Puglisi and P. Pavan, "Reliability and Performance Analysis of Logic-in-Memory Based Binarized Neural Networks," in IEEE Transactions on Device and Materials Reliability, vol. 21, no. 2, pp. 183-191, June 2021, doi: 10.1109/TDMR.2021.3075200.

[6] T. Zanotti, F. M. Puglisi and P. Pavan, "Low-Bit Precision Neural Network Architecture with High Immunity to Variability and Random Telegraph Noise based on Resistive Memories," 2021 IEEE International Reliability Physics Symposium (IRPS), 2021, pp. 1-6, doi: 10.1109/IRPS46558.2021.9405103.

[7] T. Zanotti et al., "Reliability of Logic-in-Memory Circuits in Resistive Memory Arrays," in IEEE Transactions on Electron Devices, vol. 67, no. 11, pp. 4611-4615, Nov. 2020, doi: 10.1109/TED.2020.3025271.

[8] Lanza, M., Wong, H.-S. P., Pop, E., Ielmini, D., Strukov, D., Regan, B. C., Larcher, L., Villena, M. A., Yang, J. J., Goux, L., Belmonte, A., Yang, Y., Puglisi, F. M., Kang, J., Magyari-Köpe, B., Yalon, E., Kenyon, A., Buckwell, M., Mehonic, A., Shluger, A., Li, H., Hou, T.-H., Hudec, B., Akinwande, D., Ge, R., Ambrogio, S., Roldan, J. B., Miranda, E., Suñe, J., Pey, K. L., Wu, X., Raghavan, N., Wu, E., Lu, W. D., Navarro, G., Zhang, W., Wu, H., Li, R., Holleitner, A., Wurstbauer, U., Lemme, M. C., Liu, M., Long, S., Liu, Q., Lv, H., Padovani, A., Pavan, P., Valov, I., Jing, X., Han, T., Zhu, K., Chen, S., Hui, F., Shi, Y., "Recommended Methods to Study Resistive Switching Devices", Adv. Electron. Mater. 2019, 5, 1800143. https://doi.org/10.1002/aelm.201800143 – **most cited article of 2019 in Adv. Electron. Mater.**

[9] L. Selmi et al., "Modelling nanoscale n-MOSFETs with III-V compound semiconductor channels: From advanced models for band structures, electrostatics and transport to TCAD," 2017 IEEE International Electron Devices Meeting (IEDM), 2017, pp. 13.4.1-13.4.4, doi: 10.1109/IEDM.2017.8268384.

[10] Y. Shi et al., "Coexistence of volatile and non-volatile resistive switching in 2D h-BN based electronic synapses," 2017 IEEE International Electron Devices Meeting (IEDM), 2017, pp. 5.4.1-5.4.4, doi: 10.1109/IEDM.2017.8268333.

[11] F. M. Puglisi et al., "2D h-BN based RRAM devices," 2016 IEEE International Electron Devices Meeting (IEDM), 2016, pp. 34.8.1-34.8.4, doi: 10.1109/IEDM.2016.7838544.

[12] F. M. Puglisi, F. Costantini, B. Kaczer, L. Larcher and P. Pavan, "Probing defects generation during stress in high-κ/metal gate FinFETs by random telegraph noise characterization," 2016 46th European Solid-State Device Research Conference (ESSDERC), 2016, pp. 252-255, doi: 10.1109/ESSDERC.2016.7599633. – **ESSDERC 2016 Best Paper Award**

[13] F. M. Puglisi, T. Zanotti and P. Pavan, "SIMPLY: Design of a RRAM-Based Smart Logic-in-Memory Architecture using RRAM Compact Model," ESSDERC 2019 - 49th European Solid-State Device Research Conference (ESSDERC), 2019, pp. 130-133, doi: 10.1109/ESSDERC.2019.8901731. – **ESSDERC 2019 Best Paper Award**